**DAILY ASSESSMENT FORMAT**

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| **Date:** | **05-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **Digital Design using HDL** | **USN:** | **4AL17EC035** |
| **Topic:** | **1.Verilog Tutorials and practice programs**  **2. Building/Demo projects using FPGA.** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**        **TASK 5: Implement a Verilog module to count number of 0’s in a 16 bit number in compiler.** |

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| **Date:** | **05-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC035** |
| **Topic:** | **Section 32** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **AFTERNOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**    **APPLICATION 10: Build a Data Collector Web App with Post GreSQL and Flask** |

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